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RESEARCH ARTICLE

Capacitance–Voltage Spectroscopy of Trapping States in GaN/AlGaN Heterostructure Field-Effect Transistors

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In AlGaN/GaN heterostructure field-effect transistor structures, the surface defects and dislocations may serve as trapping centers and affect the device performance via leakage current and low-frequency noise. In this paper we report results of our investigation of the trapping characteristics of SiO_2-passivated $Al_{0.2}Ga_{0.8}N$/GaN heterostructure field-effect transistors using the capacitance–voltage (CV) profiling technique. From the measured frequency dependent CV data, we identified the characteristics of the traps at the AlGaN/GaN interface adjoining the channel and on the surface along the ungated region between the gate and drain. Based on the measured data, the influence of the channel traps on the low-frequency noise spectra and the effect of the surface traps on possible leakage noise are analyzed and compared with the previous studies.

Keywords: GaN, Field-Effect Transistors, Carrier Traps, Capacitance–Voltage Spectroscopy, $1/f$ Noise, Generation-Recombination Noise.

1. INTRODUCTION

Wide band-gap nitride semiconductors continue to attract attention as the materials for novel optoelectronic and electronic devices with applications in microwave communications, power and high-speed electronics.[1–4] In addition to their wide band-gap, excellent electronic transport properties have been achieved in nitride heterostructures using the piezoelectric enhancement mechanism. The two-dimensional electron gas (2DEG) with the sheet carrier density higher than 10^{13} cm^{-2} and the room temperature mobility above 2000 cm^2/Vs can be achieved at the AlGaN/GaN interface.[5,6] GaN-based heterostructure field effect transistors (HFETs) have demonstrated a very high breakdown voltage and good power transfer ability.[7,8] However, due to the structural imperfection, a lot of dislocations and defects can be generated during material growth and fabrication. As the source of trapping states in current leakage and low-frequency noise, these defects and dislocation need to be carefully studied. For the proposed application in microwave and optical communication systems, it is important to have the device running at low flicker noise level since it contributes to the phase noise of the system and degrades its performance.[9–11] The low-frequency flicker noise characteristics can also be used for inspection of the quality of the semiconductor materials.[12,13]

The $1/f$ noise is conventionally characterized by the dimensionless Hooge parameter $\alpha = (S_R/R^2)fN$, where N is the number of the electrons, f is the frequency, S_R is the noise spectral density and R is resistance. Previous studies have shown that AlGaN/GaN HFETs fabricated on sapphire and SiC substrate can have a relatively low Hooge parameter at the level of 10^{-4} (Refs. [9–11, 14]). The low-frequency noise in GaN/AlGaN HFET displayed features characteristic of the carrier-density type fluctuations. The flicker noise in GaN-based transistors was attributed to the electron tunneling from the channel to the traps distributed through the adjoining GaN or AlGaN layers.[15,16] It has also been suggested that non-uniform trap distribution can be responsible for deviations from the $1/f$ low in the noise spectra.[9] Recently, it was reported that the flicker noise in GaN/AlGaN HFETs can be dominated by the noise produced though the dislocation leakage paths.[17] The possible mechanism includes leakage current from the gate, which delivers carriers to and from the traps located on the surface and near the dislocation lines in the barrier layer. To better understand the effects of the traps on the noise characteristics in GaN-based devices, a variety of experimental techniques should be applied.

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In AlGaN/GaN HFETs, the surface donor-like traps on top of AlGaN layer can act as sources of electrons in the channel.[18] In addition to the surface traps, the electronic traps can be found in different locations in the device structure, including the barrier or channel layers, the barrier-channel interface or the metal–semiconductor interface. The nature and formation of the trap states depend heavily on the material quality and device fabrication technology. In the cases when a passivation layer is used in the fabrication of GaN transistors, the state of the surface traps (passivated surface traps) changes from the free dangling-bond state to the passivated interface state. The latter leads to the corresponding change in the trapping processes and their effect on the transistor characteristics. Although it has been acknowledged that surface passivation technology can improve the transistor performance in many aspects, including the current level,[19] breakdown field[20] and noise figure,[17] the mechanism of the improvement and the effect of different passivation technologies, i.e., SiO_2, Si_3N_4, Sc_2O_3 or SiON, on trap characteristics and GaN/AlGaN HFET performance has not been studied in detail yet.

Capacitance–voltage (CV) profiling is a well-developed characterization technology for investigation of the carrier distribution in semiconductor heterostructures.[21] In CV measurements, the frequency dispersion provides useful information on the trap states in semiconductors.[22] In previous studies, CV profiling has been applied to determine the interface 2DEG density and distribution[23]and the trap concentration in AlGaN/GaN heterostructures.[24] In this paper, we report the CV profiling measurements at different frequencies from both the large area circular Schottky diode and the small-area gate–source and gate–drain contacts on SiO_2 passivated $Al_{0.2}Ga_{0.8}N$/GaN HFETs. From the measured frequency dependent CV profiling data, we identified the AlGaN/GaN interface traps near the channel and the surface traps along the access region between the gate and drain. The effect of the interface traps on the channel noise and the surface traps on possible leakage noise is discussed based on the extracted trapping state characteristics. The rest of the paper is organized as follows. Section 2 describes the device fabrication and measurements. Section 3 presents the measured results and analysis. The conclusions are given in Section 4.

2. DEVICE FABRICATION AND MEASUREMENTS

The $Al_{0.2}Ga_{0.8}N$/GaN heterostructure was grown on a semi-insulating SiC substrate by the metal organic chemical vapor deposition (MOCVD) technique. The growth began with a thin AlN nucleation layer and was followed by 1.2 μm undoped GaN, 50 nm undoped GaN channel, 3 nm undoped $Al_{0.2}Ga_{0.8}N$ spacer and 15 nm Si doped (6×10^{18} cm^{-3}) $Al_{0.2}Ga_{0.8}N$ barrier layers. Mesa isolated circular Schottky diode with a diameter of 100 μm was fabricated on the grown wafer for CV profile measurement. The HFET fabrication steps included mesa isolation, source and drain Ohmic contacts formation, gate Schottky contact formation and surface passivation. The mesa isolation was achieved by the ion implantation of As^+ at 75 keV and the dose of 1.27×10^{11} cm^2; As^+ at 375 keV and the dose of 4.32×10^{11} cm^2; and He^+ at 75 keV and the dose of 5.43×10^{11} cm^2. The source–drain Ohmic contacts were formed using Ti/Al/Ni/Au (200 Å/800 Å/400 Å/1500 Å) metal layers. The contact metal multilayer was deposited by the e-beam evaporator and lift-off technology, followed by 900 °C N_2 ambient rapid thermal annealing for 30 seconds to reduce the contact resistance. The contact resistivity of less than 10^{-6} Ω cm^2 was obtained using this processing method. The gate Schottky contact was formed by Pd/Au (200 Å/6500 Å) metal layers. To obtain a good Schottky junction, a proper surface treatment is required before the metal evaporation. After pattern transfer, O_2 descum and 30 s buffered oxide etchant (BOE) dip were conducted to remove residues and the thin oxide layer at the contact area. After BOE dip, the sample was cleaned by di-water rinse and N_2 blow dry. The contact metal was also deposited by the e-beam evaporator. After the above processes are finished, a 270 nm SiO_2 layer was deposited by the plasma enhanced chemical vapor deposition (PECVD) to provide surface passivation. The metal contact windows were opened with BOE etching. Devices with metallurgical gate length 1 μm, gate width 20 to 50 μm and source to drain distance 3 μm are fabricated.

The CV profiling measurements were performed using an upgraded Aglient 4284A LCR meter combined with Signatone high-frequency probe station. The oscillation frequency range of the LCR meter is from 20 Hz to 1 MHz. The DC bias applied to the gate–source (drain) was from 0 V to −6 V and the AC signal was kept at 40 mV. At each frequency, the LCR meter was carefully calibrated to compensate for the parasitic resistance from the measurement circuit. The data accumulation was automated by the LabVIEW software.

3. EXPERIMENTAL RESULTS AND DISCUSSION

Figure 1 shows the measured capacitance from the Schottky diode at 50 KHz and 1 MHz. From the data of 1 MHz measurement, we derived the apparent carrier concentration versus depletion depth ($N_{CV} - w$) profile as shown in the inset. From the charge conservation equation:[21]

$$n_s = \int_{-\infty}^{\infty} N_{CV}(w)dw = \int_{-\infty}^{\infty} n(z)dz \qquad (1)$$

The sheet carrier concentration obtained from ($N_{CV} - w$) profile is about 10^{13} cm^{-2}. The measured CV profiling data have been compared with the simulation results obtained by solving the one-dimensional Poisson–Schrodinger model.[25] In the simulation procedure,

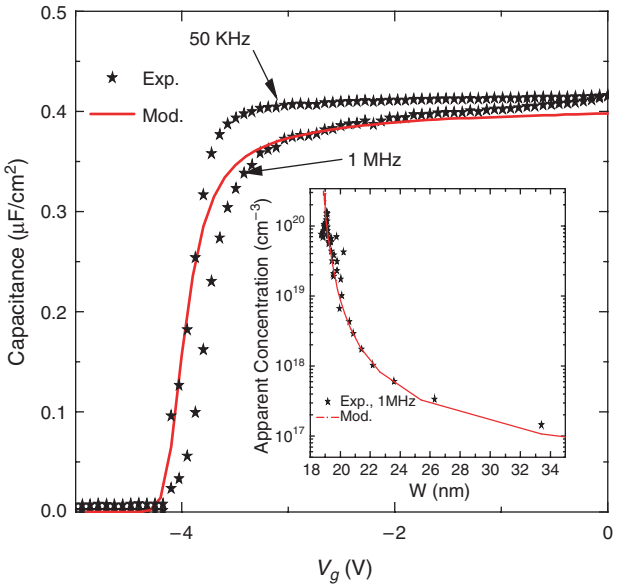

Fig. 1. The measured capacitance (points) from the circular Schottky diode at 50 KHz and 1 MHz compared with the simulated results (line) obtained from the one dimensional Poission–Schrodinger model with polarization effect included. The inset figure shows the apparent carrier concentration versus depletion depth ($N_{CV} - w$) profile derived from the 1 MHz measurement (points) and the one dimensional Poission–Schrodinger model (line).

the input AlGaN/GaN HFET structure parameters such as Al content, layer thicknesses and the doping concentration were chosen to be the same as in the fabricated HFETs structure. The polarization charge at the interface induced by the piezoelectric and strain fields is included in the simulation. The simulated CV and $N_{CV}(w) - w$ curves are shown as lines in the figure and inset respectively. The frequency dispersion of capacitance and its dependence on gate bias is demonstrated in the figure. The threshold voltage V_{th} of our material is about -3.8 V. It can be seen that the most significant dispersion appears when the gate is biased before the threshold. In the region where the channel is pinched-off (below -4 V) or fully open (close to 0 V), the measured capacitance varies little with the frequency. The observed dispersion shows the response of the trap states in the HFET structure to the applied AC oscillations.[24] The shape of the dispersion and the bias potential suggest that the location of the traps is possibly barrier layer near AlGaN/GaN interface or in the 2DEG channel. The extraction of the trap state characteristics follows the method developed for MOS structure.[26] The measured capacitance $C_{g,ch}$ can be written as

$$(C_{g,ch})^{-1} = (C_b)^{-1} + (C_{ch} + C_{it})^{-1} \tag{2}$$

where C_b is the barrier capacitance, C_{ch} is the channel modulation capacitance, and C_{it} is the trap capacitance. The barrier capacitance, which approximately equals the capacitance at zero bias, is insensitive to the frequency variations. It has been shown that the traps adjoining the depleted channel demonstrate a multi-level energy distribution.[24] At the specific gate bias, C_{it} can be extracted from the measured data using Eq. (2) and from which the density of trap energy level and time constant can be estimated using the equations

$$D_{it} = \frac{C_b}{q}\left(\frac{C_{lf}/C_b}{1 - C_{lf}/C_b} - \frac{C_{hf}/C_b}{1 - C_{hf}/C_b}\right) \tag{3}$$

and

$$C_{it} = \frac{D_{it}}{q}\frac{1}{2\pi f t \tan(2\pi f t)} \tag{4}$$

where D_{it} is the density of the trap energy levels, C_{if} and C_{hf} are the measured low and high frequency capacitances, respectively, and τ is the trap time constant. From the measured bias dependent CV data, the values of D_{it} from $\sim 10^{11}$ cm^{-2} eV^{-1} to $\sim 5 \times 10^{12}$ cm^{-2} eV^{-1} with the time constants at $\sim\mu$s level can be obtained.

In addition to the hetero-interface and the channel layer, another major source of the traps, which might contribute to the noise, comes from the ungated or passivated surface. The surface traps may show their effect in the fringe capacitance between the gate–source and the gate–drain contacts. When a bias is applied between the gate and drain, the depletion region is formed by: I, the channel area underneath the gate, and II, the area between gate and drain. Based on the effective gate-length extraction theory, the measured capacitance is composed of three parts:[27]

$$C_{tot}(V_{gd}) = C'_{channel}(V_{gd}) + C_{fringe}(V_{gd}) + C_{pad} \tag{5}$$

where C_{tot} is the total measured capacitance, $C_{channel}$ is the capacitance component from the gate covered channel area as defined in Eq. (2), C_{fringe} is the fringe capacitance from the ungated area between the gate and drain and C_{pad} is the pad capacitance between the electrodes. V_{gd} is the bias voltage between the gate and drain. It has been shown that, for transistors with the same pad patterns and fabrication process, the pad capacitance is nearly constant and independent of gate bias, and $C_{channel}$ and C_{fringe} varies linearly with the gate width W. Therefore one can extract the pad capacitance using

$$C_m(W) \approx C_{l,ch+fr} \cdot W + C_{pad} \Rightarrow C_m(W = 0) \approx C_{pad} \tag{6}$$

from different gate width measurements. In Eq. (6), $C_{l,ch+fr}$ is the capacitance from both the gated channel and ungated access area normalized to the unit gate length. Following the same principle, the effective gate length $L_{g,eff}$, which is dependent of bias level, can be extracted by

$$L_{g,eff}(V_{gd}) = \frac{C_{tot}(V_{gd1}) - C_{tot}(V_{gd2})}{W \cdot [C_{channel}(V_{gd1}) - C_{channel}(V_{gd2})]} \tag{7}$$

with the conditions that

$$0 > V_{gd}, V_{gd1}, V_{gd2} > \frac{V_{th}}{2} \quad \text{and} \quad V_{gd1} - V_{gd2} \ll \frac{V_{th}}{2} \tag{8}$$

Figure 2(a) shows the measured gate–drain capacitance as the function of the gate bias from the 20 μm gate and 50 μm gates at 1 MHz. The C_{pad} extrapolated from

the small gate bias of the two measurements is about 40 fF. Once C_{pad} is known and $C_{channel}$ is obtained from the circular Schottky diode, the fringe capacitance can be extracted from the measured gate–drain capacitance using Eq. (4). The extraction method is described in Ref. [27]. Here, we show the extraction results for the 20 μm gate in Figure 2(b), which shows the C_{tot}, $C_{channel}$, and C_{fringe} values as the functions of the gate–drain bias V_{gd}. The peak on the C_{fringe} curve, which may not appear in reality, is an artifact of the way it has been calculated: near the pinch-off, the shape of the depletion region is somewhat round while the non-uniformity is included in C_{fringe}.[27] From this figure one can also observe the pinch-off-like behavior of the extracted C_{fringe}. A possible explanation of this is the surface-fixed charge depletion effect.[26] It is interesting to note that such pinch-off-like behavior of the fringe capacitance is essentially identical to the second gate effect suggested by Vetury et al.[28] Figure 2(c) shows the extracted effective gate length as a function of bias. It can be seen that at effective gate length varies around the metallurgical

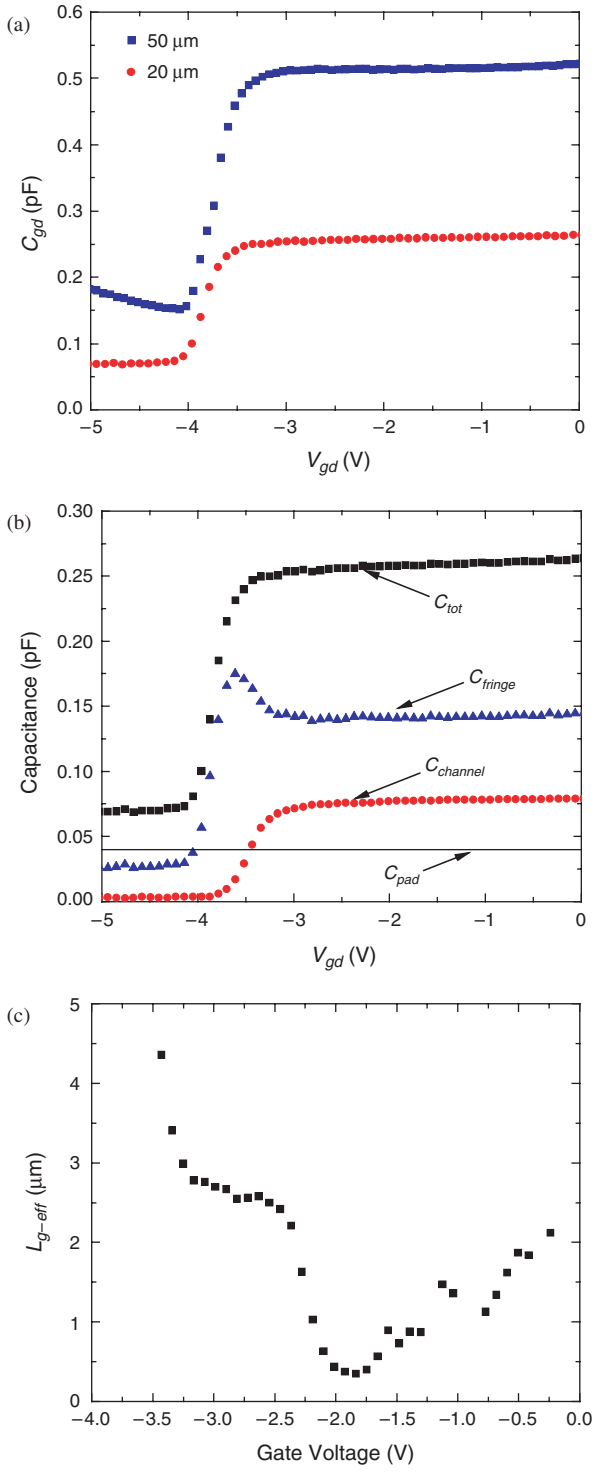

Fig. 2. (a) Capacitance between the gate–drain area measured from 20 μm gate and 50 μm gate at 1 MHz. (b) Measured capacitance C_{tot}, channel capacitance $C_{channel}$ obtained from the circular diode, and the extracted fringe capacitance C_{fringe} as the functions of the gate–drain voltage V_{gd}. (c) The extracted effective gate length as a function of gate bias.

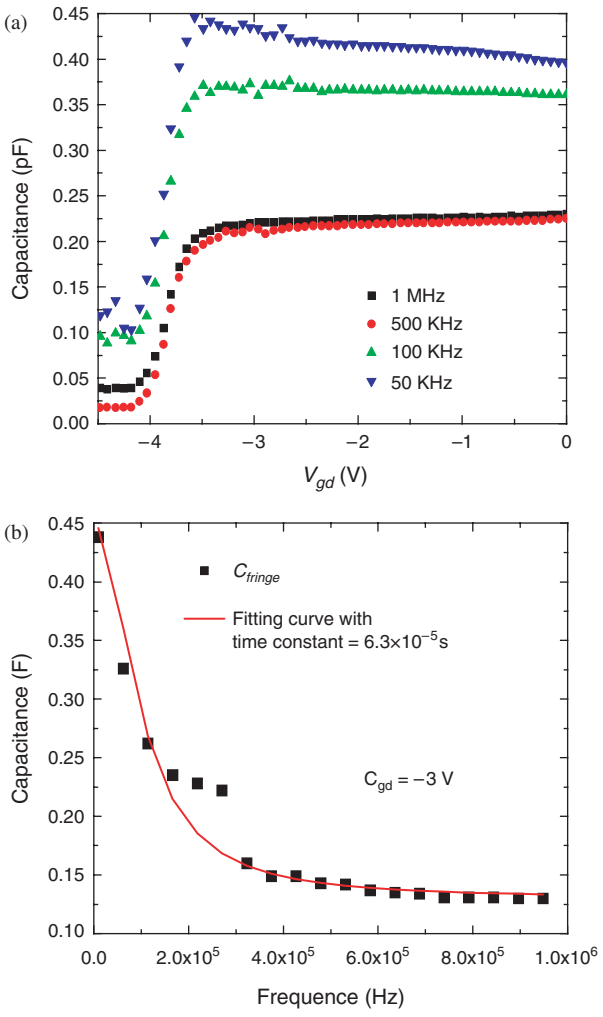

Fig. 3. (a) CV profiles of the gate–drain area at several oscillation frequencies (50 KHz, 100 KHz, 500 KHz, and 1 MHz) measured from the 20 μm gate. (b) Frequency sweep CV measurement data from 50 KHz to 1 MHz at the gate bias of −3 V. The fitting of the measured data using Eq. (9) gives time constant $\tau = 63$ μs and $D_{it} = 6 \times 10^{12}$ cm^{-2} eV^{-1}.

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gate length (1 μm) at low gate bias, may become much larger when the gate voltage approaches threshold.

The example of C_{fringe} shown in Figure 2 is obtained from the measured capacitance at 1 MHz. Following similar procedure one can extract the C_{fringe} from frequency dependent CV measurement and obtain the trap status about the defects/dislocations near the surface. Figure 3(a) shows a typical gate–drain CV profiling data measured from the 20 μm gate at frequencies 1 MHz, 500 KHz, 100 KHz, and 50 KHz. Appreciable dispersion is observed in the measured data. The pattern of the gate–drain capacitance dispersion is quite different from the circular Schottky diode shown in Figure 1. Taking into consideration the insensitivity of barrier pad capacitances to the oscillation frequency and the relatively small dispersion in the channel capacitance, it is reasonable to attribute the observed frequency dispersion to the traps in the fringe capacitance, i.e., the surface states in the access region. To further identify the origin of the traps, we conducted the frequency sweep of the capacitance at the different fixed gate bias. Figure 3(b) shows the sweep data from 50 KHz to 1 MHz at gate bias of -3 V. It is interesting to see that the frequency sweep curves at different biases can be fitted with a single trap response given by the formula[29]

$$C_{\text{m}} = C_{\infty} + \frac{D_{\text{it}}/q}{1+(2\pi f\tau)^2} \tag{9}$$

where C_{m} is the measured capacitance and C_{∞} is the constant capacitance at high frequency. The fitting results are shown as the solid line in Figure 3(b). From the fitting, the trap state with the time constant $\tau = 63$ μs and $D_{\text{it}} = 6\times10^{12}$ cm^{-2} eV^{-1} is obtained. This result suggests that the traps are likely in the ungated region between the gate–drain, possible resulting from the SiO_2 passivation layer.

The CV measurement demonstrated that the traps adjoining the channel and at the ungated surface have the time constant at the range of μs and that their density and activation energy depend on the bias energy level. These trapping states can manifest themselves in the noise measurements at different frequencies and bias conditions. Several studies have shown that the carrier number fluctuation due to the carrier trapping and detrapping is the major source of noise in GaN HFET channel.[9–11, 16, 30] The generation-recombination (g-r) bulge, a typical indication of number fluctuation mechanism, has been observed in the noise spectra of GaN/AlGaN HFETs.[30, 31] The g-r bulges, according different studies, are normally observed at the frequencies from several KHz. To understand the effect of the measured μs level traps on the transistor noise, we simulated the noise spectra in GaN/AlGaN HFETs using the number fluctuation model. Assuming a trap state with specific spatial distribution $N_s exp(-ay)$ and the time constant $\tau_s = 1$ μs located adjacent to the channel within thickness d, the normalized noise density $S_{I(V),\text{Norm}}$

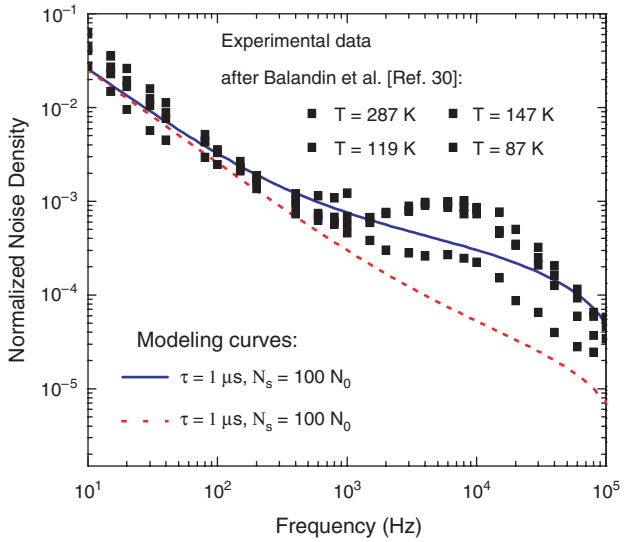

Fig. 4. The simulated noise spectra for distributed traps with the $\tau_s = 1$ μs and $N_s = 100N_0$ (solid line), and $\tau_s = 1$ μs and $N_s = 10N_0$ (dashed line), compared with the experimental data (points). The experimental values are after Balandin et al.[30]

can be calculated as[32]

$$S_{I(V),\text{Norm}} = \int_0^d [N_s \exp(-ay) + N_0] \frac{\tau_s \exp(ay)}{1+(2\pi f\tau_s)^2 \exp(2ay)} dy \tag{10}$$

where N_0 is the background uniform trap distribution, τ_s is the specific trap time constant, a is at the scale of the inverse of the atomic distance, N_s is the specific trap density, a parameter dependent on the material structure and the fabrication technology. In the simulation, we consider two cases, $N_s = 100N_0$ and $N_s = 10N_0$ to elucidate the influence of the trap densities on the noise spectra.

In Figure 4 the solid lines are the simulated noised spectra of the two cases. It can be seen that, when $N_s \gg N_0$, the traces of the bulge is apparent even when f is smaller than 1 KHz. While in the case $N_s = 10N_0$, the trace of bulge is indicated when f is higher than 10 KHz. On the other hand, the large trap density results in the higher noise level near the knee frequency. To compare with the experimental noise data, we included in Figure 4 the measured noise densities at different temperatures from AlGaN/AlN HFET reported in Ref. [30]. The data are normalized at certain low frequency values and shown as points in the figure. The comparison of the simulated and measured results indicate that the traps with μs time constants and densities determined from the CV profiling indeed contribute to the flicker noise in the GaN HFETs.

The effect of the traps on the low-frequency noise can also be seen in the noise density (S_I) dependence on the effective gate bias V_G. It has been found that the main contribution to the noise in GaN/AlGaN HFETs can come from either the channel or ungated region between the source and drain, under either the channel or the ungated region resistance domination.[10] However, at

certain frequencies, $S_I - V_G$ does not follow either V_G^{-1} or V_G^{-3} dependences often observed in GaN HFET noise. It has been suggested that the surface-trap-dislocation related leakage paths cause the deviation.[17] The deviation of the V_G dependence reported in Ref. [17] is obtained at about 10 KHz, which is within the range of frequencies for the $\tau = 63$ μs surface trap determined in this study. It should be noticed though that the passivation layer used in Ref. [17] is Si_3N_4 while the one used in this study is SiO_2. At present time, no detail study on the surface related leakage noise has been conducted.

4. SUMMARY

We conducted frequency dependent CV measurements on both circular Schottky diode and HFETs fabricated on $Al_{0.2}Ga_{.8}N$/GaN heterostructure grown on SiC substrate. From the CV profiling data we identified that the traps adjoining 2DEG channel have the density of the trap energy level D_{it} from $\sim 10^{11}$ cm^{-2} eV^{-1} to $\sim 5 \times 10^{12}$ cm^{-2} eV^{-1} and the time constants in the μs range. From the measured gate–source capacitance the fringe capacitance between the gate–drain access region is extracted, and a single level trap with $\tau = 63$ μs and $D_{it} = 6 \times 10^{12}$ cm^{-2} eV^{-1} is derived from the measured fringe capacitance dispersion. Using the trap parameters obtained from the CV data, we simulated the noise spectra of GaN/AlGaN HFETs with the specific $\tau_s = 1$ μs trap and compared the results with previous experimental studies.

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